REMARKS

This is in full and timely response to the Official Action mailed February 24, 2006. Reconsideration and reexamination are respectfully requested. A petition to extend the time for this response to within the second extended month accompanies this submissioin.

Priority Claim

It is noted with appreciation that the certified copies of the priority documents have been received and acknowledged by the Examiner.

Drawings

It is also noted with appreciation that the drawings are accepted by the Examiner.

Information Disclosure Statement

The Information Disclosure Statement filed on October 20, 2004 has been considered by the Examiner as noted by the initialed PTO 1449 form.

Claims

Claims 1 to 12 were pending in the application as initially examined. All of the claims were initially rejected on the basis of Hashizume along or in combination with Cavaliere '254 (claims 4, 9, and 12) or in combination with Tamamura '316 (claims 6, 7). These rejections are respectfully traversed.

Without indicating agreement with or acquiescence in the statements of the rejection, claims 1 to 8 are revised to better distinguish over Hashizume as originally applied. Specifically, Hashizume arguably discloses a semiconductor integrated circuit with a test circuit for readily subjecting the IC to a direct current test (col. 1, lines 8 to 14). The DC characteristic test is described at col. 1, lines 24 to 30. A boundary scan test is further described at col. 1, lines 31 to 44.

The circuit of the Applicant's invention uses a scan pattern provided to a scan chain between a scan in terminal and a scan out terminal, wherein a plurality of flip-flops are provided between those terminals to perform logic testing responsive to the scan pattern. A scan mode terminal provides a scan mode signal for switching the internal logic circuitry between the normal operation state and a scan operation state that includes the recited test mode. The recited interplay between a scan pattern signal in the circuit and the scan mode signal with respect to resetting the plurality of flip-flops when transitioned responsive to the scan mode is, insofar as Hashizume teaches, unique.

Background Consideration

A starting point for the problem and solution analysis that lends itself quite well to this subject matter is the specification at pages 1 and 2, relative to prior art Fig. 4, and the associated problems recited at pages 2 and 3, leading to the solutions noted at the bottom of page 3 to page 7. The examiner is invited to review this disclosure for its applicability to the rejections phrased and responded to in this response.

Mapping

The examiner has provided a significant amount of information to sift through when considering the stated rejection by his citations from the references and in particular from the Hashizume reference. However, a difficulty in applying the rejection to the pending claims is that the claim limitations are not mapped specifically in the manner contemplated by the MPEP. As the application of Hashizume is understood, there is no such interplay as is claimed between a signal equivalent to the recited scan mode signal and a signal equivalent to the scan pattern signal as is recited in the terminal paragraph of claim 1 as amended.

Amendments to Claims

Claims 1 to 8 are amended to depend on or through claim 1 as amended so that the theme established is continued. Claim 4 further recited memory means against which a combination of Hashizume and Cavaliere was applied. As amended, claim 4 continues to be patentable because it

depends from claim 1, and for the further reason that it stands in its own right. Furthermore, the reasons for the motivation to make the modification stated at the top of page 5 of the Action are more in the nature of conclusions arising from the combination rather than findings for making or motivating the making of the combination.

Still further, the subject matter of original claim 4, with some additional changes is restated in claim 14. To the extent that the rejection of original claim 4 may still be thought to apply, reconsideration of all of the language in claim 14 and claims dependent thereon is solicited, along with a reassessment of the reasons for making the modification.

Claims 9 and 12 are patentable over the combination stated because of the flawed reasons for motivating the combinations posed. Accordingly, reconsideration is requested without modification. It is particularly noteworthy that no additional reasons for motivating a modification of Hashizume according to Cavaliere are advanced on page 5 of the Action relative to the specific terms of claims 9 and 12.

Claim 10 is made dependent as a method of testing the invention of claim 1, while claim 11 is made dependent as a method of testing the invention of claim 6.

Added claims

Claim 13 is added to recite an edge detecting feature described in the specification in a claim dependent on amended claim 1.

Finally, new claims 19 to 23 are added to recite, without reference to a means plus function, the circuit of Fig. 1 as described in the specification as filed at pages 8 to 12.

Conclusion

Claims 1 to 23 are patentable over the art cited for the reasons advanced in this response.

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Respectfully submitted,

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